

NEAR UV LED CHIP STANDARD SPECIFICATIONS

Part No. SLOA14-VL

PREPARED BY 3DZ LTD		
Engineer		Qualified
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APPROVED BY CUSTOMER		



1. APPLICATION

This specification is applied to “ITO coated Violet LED chip products”

2. PART Number : SLOA14-VL

3. PHYSICAL CHARACTERISTICS

3.1 Materials

- Substrate : Sapphire
- Epitaxial Layer : GaN based Alloy
- Backside : Metal Reflector Coated

3.2 Electrode

- Transparent Electrode : ITO
- Anode : 100 μ m with Au alloy
- Cathode : 100 μ m with Au alloy

3.3 Mechanical Data

- Chip Size : 350 μ m x 350 μ m (\pm 25 μ m) (14 mil)
- Chip Thickness : 80 μ m typical

3.4 Chip Appearance : (refer to “attached 1”)

4. ELECTRICAL AND OPTICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Item	Symbol	Maximum Rating	Unit
DC Forward Current	I _F	30	mA
Pulse Forward Current	I _{FP}	100	mA
Reverse Voltage	V _R	5	V
Operating Temperature	T _{opr}	-30 to +85	°C
Storage Temperature	T _{stg}	-40 to +100	°C

4.2 Electrical and Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Forward Voltage	V _F	I _F = 20mA	3.0	3.6	4.0	V
		I _F = 10uA	2.0	-	2.7	V
Reverse Current	I _R	V _R =5V	-	-	1.0	uA
Peak Wavelength	W _P	I _F =20mA	Refer to Rank Information			nm
Radiant Intensity*	I _E	I _F =20mA				mW

* Above radiant intensity is relative value on chip level, not absolute, depends on customer package types.

4.3 Rank Information

WP I _E (Arb.)	400.0nm~ 405.0nm	405.0nm~ 410.0nm	410.0nm~ 415.0nm	415.0nm~ 420.0nm	420.0nm~ 425.0nm
100 ~ 120 ~ 140	405L-SL-A8	405H-SL-A8	415L-SL-A8	415H-SL-A8	425L-SL-A8
	405L-SL-A9	405H-SL-A9	415L-SL-A9	415H-SL-A9	425L-SL-A9
140 ~ 160 ~ 180	405L-SL-A10	405H-SL-A10	415L-SL-A10	415H-SL-A10	425L-SL-A10
	405L-SL-A11	405H-SL-A11	415L-SL-A11	-----	-----
180 ~ 200 ~ 220	-----	405H-SL-A12	415L-SL-A12	-----	-----
	-----	-----	415L-SL-A13	-----	-----

Note : 1) Ambient condition for measurement is in range of 22 \pm 3°C.

2) Peak wavelength includes an error of \pm 2nm.

3) 3DZ provides relative radiant intensity (I_E) data by 3DZ LTD standard chip probing system.

4) GaN based LED is sensitive to electrostatic damages. Please take appropriate precautions

5) All samples are 100% tested and sorted. User can be consulted on special specification.

6) Above specifications can be revised without notification by 3DZ LTD.

5. GUARANTEED STORAGE AND OPERATING TEMPERATURE

- 5.1 Single Chip Storage Temperature
-40°C ~ 100°C
- 5.2 Storage Temperature of Product
Room temperature less than 30°C
- 5.3 Guaranteed Maximum Temperature at Assembly
350°C, less than 30 min.
- 5.4 Storage Term of Product
6 months in storage box under inert ambient

6. INSPECTION PROCESS

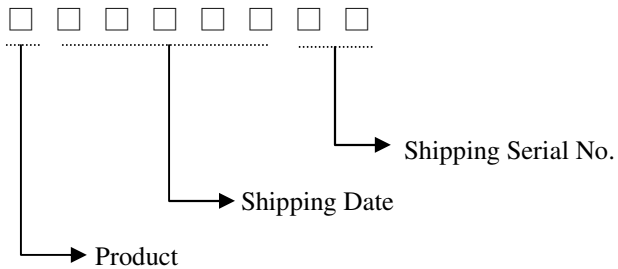
- 6.1 Electrical and Optical Characteristics
In compliance with article 4, all of chips are tested and sorted for V_F , I_R , I_E and λ_p .
- 6.2 External Appearance
In compliance with the external appearance inspection criteria (refer to “attached 2”), visual inspection is conducted by optical microscope for all pieces of chip. The chips which not conformed to criteria are removed from products. Guarantee level is based on “MIL-STD-105D Level II AQL=0.4%”.

7. PACKING STANDARD

- 7.1 Minimum Number of Chips for Array Sheet
200pcs or more
- 7.2 Chip Array Sheet Dimension
185mm X 185mm (+/-5mm)
- 7.3 Chip Array Area
40mm x 60mm (Max.)
- 7.4 Chip Arrangement Spacing
150um ~ 300um
- 7.5 Packaging
Electrostatic shielded packing by thermal pressure sealer.

8. LOT NUMBERING

8.1 Shipping Lot Number



9. CERTIFICATION

9.1 Sheet Label (refer to “attached 3”)

For every chip array sheet, label sheet including part number, rank number, lot number, quantity and characteristic data is attached individually.

9.2 Packing List (refer to “attached 4”)

Packing list includes information of shipping lot number, quantity and shipping date etc.

9.3 Certificate Sheet (refer to “attached 5”)

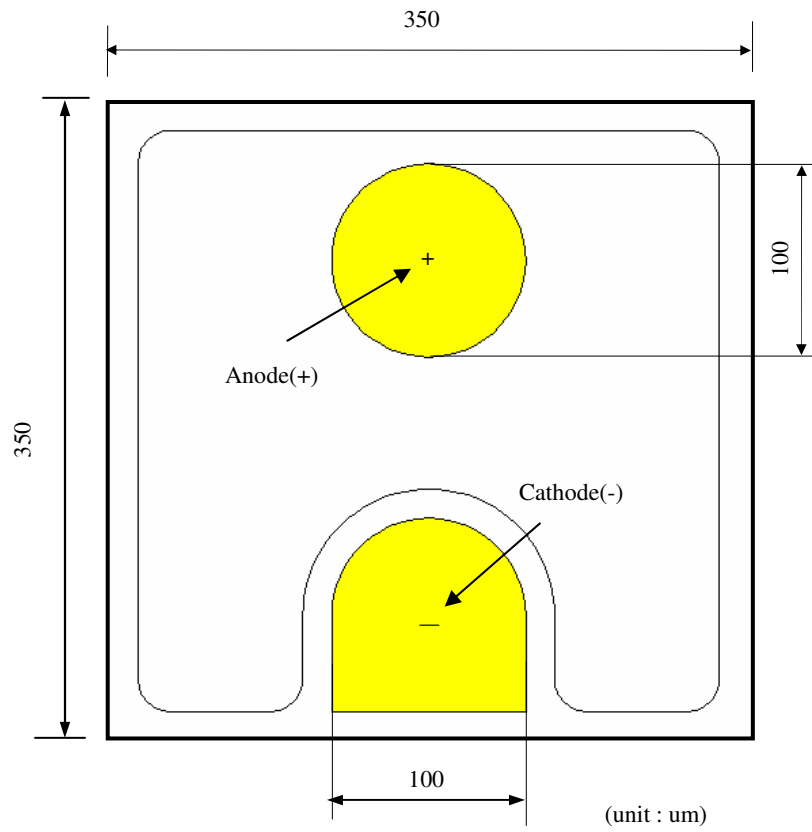
Certificate Sheet includes information of process lot and characteristic data.

10. REMARKS

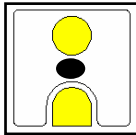
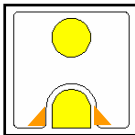
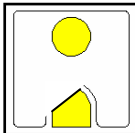
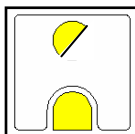
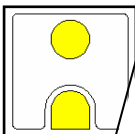
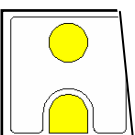
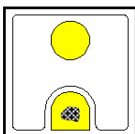
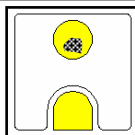
If any of complaint is raised for products or technologies which are not described in this specification, both parties shall meet and clearly establish the causes of the complaint before taking any action.

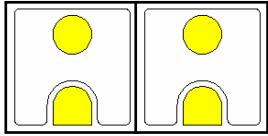
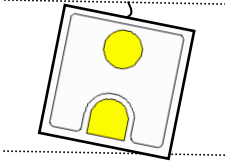
(attached 1)

CHIP APPEARANCE



EXTERNAL APPEARANCE INSPECTION CRITERIA

Items	Evaluation Standard	Example
Surface Contamination	Surface dirt on the light - emitting surface, and junction to be 20% or less of the chip area	
Damage of P-Side Transparent Electrode	Damage of P-Side Transparent Electrode to be 20% or less in terms of the chip area ratio	
Partially Peeled Pad Metal	The peeled portion of the N-pad to be 25% or less of the N-pad area	
	The peeled portion of the P-pad to be 25% or less of the P-pad area	
Chipping / Bad Cut	N-Side and /or P-Side electrode not chipped off	
	P-N Junction area not to be damaged	
Pad Contamination	Surface dirt on the N-pad surface to be less 10% of the chip area	
	Surface dirt on the P-pad surface to be less 10% of the chip area	

Items	Evaluation Standard	Example
Twin / Triplet	Chip should not be two or more per placement.	
Rotation	Chip Rotation to be less 10 degrees of the standard sorted chips	
Displacement	Chips will be aligned on the tape to within 100µm	